REMARKS / ARGUMENTS

This Amendments and Response to Office Action is filed in response to the Office Action of October 5, 2004. Presently, Claims 1-10 stand rejected under 35 U.S.C. § 112, ¶ 2, as being indefinite due to lack of antecedent and presence of ambiguity. The drawings and the claims further stand objected due to minor informalities.

In addition, claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,249,145 issued to Tanaka *et al.* ("Tanaka *et al.*"). Moreover, claims 2-9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka *et al.* in view of U.S. Patent No. 5,917,339 issued to Kim ("Kim").

New claims 11-20 are added for consideration without adding any new matter. With entry of the above amendments and consideration of the reasons stated below, Applicant respectfully submits that the objections and rejections set forth in the outstanding Office Action are overcome.

I. Objections to the Drawings

The drawings stand objected because the "resistor" as recited in claim 5 is not shown. The drawings are amended to show this feature and no new matter is added. New Fig. 5A is the original Fig. 5, and new Fig. 5B is added to show the resistor. By way of this amendment, Applicant submits that the objection has been overcome, and withdrawal of the objection is respectfully requested.

II. Rejection of claims 1-10 under U.S.C. § 112, ¶ 2

Claims 1-10 stand rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite. Applicant submits that these amendments have overcome the rejection of claims 1-10 under U.S.C. § 112, ¶ 2, and the withdrawal of the rejection is respectfully requested.

III. Rejection of Claims 1 as Being Anticipated by Tanaka *et al.*

Claim 1 currently stands rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by Tanaka *et al.* In light of the claim amendments made herein and the reasons stated *infra*, Applicant respectfully traverses the anticipation rejection because Tanaka *et al.* fails to disclose each and every element of the claim.

The subject application is directed to overcome the drawbacks in conventional level shifter circuitry when the voltage difference between the shifted signals becomes relatively large. According to one aspect of the present invention, the PMOS and NMOS transistors in the basic shifter are fabricated of comparable physical scales. To accomplish the above objective, with reference to Fig. 2 of the subject application, the dynamic CMOS level shifter circuit apparatus uses a power-down control signal (*PWD*) at the gate terminal 231 of the PMOS transistor 230 for a specified period of time during operation. As the power-down control signal *PWD* is asserted, the power to the PMOS transistors 211 and 221 in the basic shifter 100 of Fig. 2 is cut off for a sufficient period of time when the NMOS transistors 212 and 222 of the basic shifter 100 settle to their state transition.

In the subject application, the provision of the power-down control PMOS (NMOS) transistor and the power-down control signal advantageously eliminates the excessive transition power and device size asymmetry, as shown by the waveform in Fig. 3 of the subject application.

The duration (T1-T2) of the power-down control signal (*PWD*) can be flexibly modified in the event that the desired output voltage level for the level shifter circuit apparatus is changed (for example, from 5V to 12V). Therefore, the level shifter circuit apparatus according to the subject application can be easily optimized to provide output voltages of different levels.

Takana *et al.* discloses a level shift circuit and the level shift circuit shown in Figure 12 thereof has an output fixing function. "When the power supply of the circuit block 510 is turned off, no through-current flows between the power supplies of circuits 516 when input IN1 is set to an appropriate level, thereby stabilizing the output OUT0." *See* Takana *et al.*, col. 8, lines 32-40. Simply put, the control signal IN1 is used in the event that the circuit block 510 is turned off and is intended to turn off the whole level shift circuit to stabilize the output OUT0 and to reduce power consumption.

On the other hand, in the subject application, the power-down control signal (PWD) changes to a high state for a predetermined period of time when the signal of the first logic family changes to a high state (as can be seen in Fig. 3 of the subject application). The predetermined period of time is a period of time sufficient for the first and second NMOS transistors to settle to their respective state transition. Moreover, during the predetermined period of time, the first and second PMOS transistors are cut off from the power supplied thereto.

Takana *et al.* fails to teach or even suggest such features as "the power-down control signal is switched to a high state for a predetermined period of time when the signal of the first logic family changes state," and "the power-down control signal controls the gate terminal of said power-down control PMOS transistor to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition," as recited in amended claim 1. For at least these reasons, Applicant

respectfully submits that the anticipation rejection is inadequate, and its withdrawal is respectfully solicited.

VI. Rejection of Claims 2-10 as being unpatentable over Tanaka *et al.* and Kim

With respect to claim 2, the Examiner stated that the subject application is obvious in view of the combination of the level shift circuit (516) in Figure 12 of Takana *et al.* and the first and second inverters (15, 16) in Fig. 2 of Kim.

In claim 2 of the subject application, the provision of two serially-connected inverters prevents signal ambiguity when complementary outputs are required. Through this line of reasoning, the level shift (516) in Figure 12 of Takana *et al.* and the first and second inverters (15, 16) in Fig. 2 of Kim are not combinable. The level shift (516) in Figure 12 of Takana has only one output OUT0 and the signal IN1 in Figure 12 is intended to block the power from supplying to the level shift (516). The first and second inverters (15, 16) in Fig. 2 of Kim are powered by the core power CVDD. The addition of the first and second inverters of Kim to the output stage of the level shift (516) of Takana *et al.* will defeat the intended purpose of Takana *et al.*, i.e. providing a fixed output. The introduction of the two inverters will inevitably connect the output port of the level shift circuit to the power source.

There is also no suggestion to combine the level shift circuit (516) of Takana and the inverter(s) of Kim. The level shift circuit (516) of Takana has only one output, and there is no motivation to add two inverters to the single output thereof to prevent signal ambiguity. For at least these reasons, Applicant respectfully submits that the rejection is inadequate, and its withdrawal is respectfully solicited.

With respect to claim 3, for at least the same reasons as those stated for claim 2, the

withdrawal of the rejection to this claim is respectfully solicited.

With respect to claims 4 and 5, by virtue of their respective dependency upon claim 3, dependent claims 4 and 5 should also be patentable over the prior art references.

With respect to claim 6, for at least the same reasons as those stated for claim 2, the withdrawal of the rejection to this claim is respectfully solicited.

With respect to claim 7, by virtue of its dependency upon claim 6, dependent claim 7 should also be patentable over the prior art references.

With respect to claim 8, the October 5, 2004 Office Action states that this claim is obvious in view of Figs. 6 and 12 of Takana *et al.* and Fig. 2 of Kim. However, the combination thereof cannot achieve the intended purpose of the subject application, as claimed in claim 8.

The object of the subject application is to take advantage of PMOS and NMOS transistors with comparable physical scales even when the voltage difference between the shifted signals becomes relatively large (for example, 3.3V vs. 12V). If the voltage difference between the shifted signals becomes excessively large, the PMOS transistor 660 can be utilized to limit the current flowing through the PMOS transistors 211 and 221, allowing the PMOS and NMOS transistors to have comparable physical scales.

The level shift circuit of Takana *et al.* shown in Figure 6 has an additional PMOS transistor 306 as a current source. "The PMOS transistor 306 contributes to an area increase, keeping the input capacitances respecting the input signals from increasing." *See*, Takana *et al.*, col. 6, lines 25-48. This design is suitable for small voltage operation, (conversion from 1.2 to 3.3V and vice versa). Therefore, the current limiting function of the PMOS transistor 306 is achieved by fabricating a PMOS with reduced gate width. This is contrary to the object of the

subject application.

Moreover, the combination of the Fig. 6 and Fig. 12 of Takana also fails to teach the prominent feature of claim 8: "the power-down control signal is switched to a high state for a predetermined period of time when the signal of the first logic family changes state," and "the power-down control signal controls the gate terminal of said power-down control PMOS transistor to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition," as recited in amended claim 8. For at least these reasons, Applicant respectfully submits that the rejection is inadequate, and its withdrawal is respectfully solicited.

With respect to claim 9, by virtue of its dependency upon claim 8, dependent claim 9 should also be patentable over the prior art references.

With respect to claim 10, for at least the same reasons as those stated for claim 1, the withdrawal of the rejection for this claim is respectfully solicited.

V. Addition of New Claims 11-20

New claims 11-20 are added to cover additional scope of the invention without introduction of new matters. Consideration and allowance of those claims are respectfully requested.

CONCLUSION

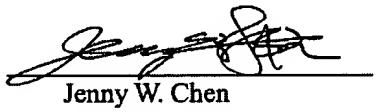
For at least the foregoing reasons, it is believed that all of pending claims 1-20 of the present application patently define over the prior arts and are in proper condition for allowance. Because this filing is submitted within the three-month deadline, no Petition for Extension of

Time is required.

Furthermore, because this filing adds new claims 11-20, additional claim fees are accounted in the transmittal letter. In the event, however, that additional fees are required to complete this filing, Commissioner is authorized to deduct any deficiencies from Deposit Account 13-0480, Attorney Docket No. 87157656.242004. If the Examiner has any questions regarding this filing or the application in general, the Examiner is invited to contact Applicant's attorney at the below-listed telephone number.

Respectfully submitted,

Date: January 4, 2005



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CLAIM DEPENDENCY CHART

Application Number: 09/765966
Filing Date: 1/19/01
Applicant(s): LinKai Bu et al.

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT		AFTER THIRD AMENDMENT		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend
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